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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,742	06/20/2003	Chu-Chin Hu	LA-7452-101	5997

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EXAMINER	
NGUYEN, HOA CAO	
ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,742	HU, CHU-CHIN	
	Examiner	Art Unit	
	Hoa C. Nguyen	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,7-12,17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,7-12,17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1 pg*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The request filed on 3/13/06 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on parent Application No. 10/600742 is acceptable and a RCE has been established. An Action on the RCE follows.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 and 7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Kimura et al. (US 6,806,428).

Regarding claim 1, as shown in figures 6(a)-6(i), Kimura et al. disclose a library core for embedded passive components comprising:

(a) An insulating core layer 31 (resin substrate, column 4, lines 18-19) having an upper and lower surface opposed to the upper surface;

(b) a plurality of openings 35 (penetration holes, column 4, lines 22 and 28) penetrating therethrough;

(c) the openings are filled with capacitive material 37 (chip capacitor, column 4, line 31 and see examiner remarks below); and

(d) a plurality of conductive traces 34 (circuit pattern, column 4, line 35) formed over the upper and lower surfaces of the core layer and fully covered the capacitive

material (see other embodiments in figures 1, 7, 8 and 11 that also show circuit traces 4a), wherein the conductive traces are electrically interconnected to the capacitive material as well as partly used as parallel sheets onto the capacitive material to form capacitors embedded in the core layer.

Examiner remarks: It is noticed that a number of openings 35 are for embedded capacitors 37, as clearly shown in the figures. The capacitor 37 (chip capacitor) has two electrodes 37a and a capacitor material formed between. Therefore, the capacitor clearly discloses the capacitive material.

Regarding claim 7, Kimura et al. disclose a plurality of conductive vias 33 (through-hole, column 4, lines 22-25) for interconnecting the conductive layers on the upper and the lower surfaces of the core layer.

Regarding claim 8, Kimura et al. disclose the library core with the patterned conductive traces that are fabricated in a semiconductor packaging substrate (module component, see column 1, lines 6-9) or printed circuit board (circuit board, see the abstract and also column 1, lines 46-48).

Regarding claim 9, as shown in figure 1, Kimura et al. disclose an insulating layer 5 formed over the conductive traces 4a and so forming a circuit layer on the insulating layer. Conductive vias 9 allows connections between layers and so forming a multi-layer circuit board (see column 2, lines 45-60).

Regarding claims 10, as shown in figure 1, Kimura et al. disclose an IC chip 7 mounted on the multi-layer circuit board and electrically coupled to the conductive traces 4a, 4b, and 4c. The multi-layer circuit board with mounted IC chip 7 is inherently

a fabrication in a flip-chip semiconductor packaging substrate, because as seen in figure 1, the IC chip 7 is faced down, see column 2, lines 54-58.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. (US 6806428) in view of Okabe et al. (US 6,757,178).

Kimura et al. disclose every limitation as shown in claims 1 and 9 above but failed to disclose the multilayer circuit board, which is fabricated in a wire-bonding semiconductor packaging substrate.

Okabe et al. disclose a multi-circuit board for embedded passive components 52 and 53 intentionally applicable to a wire-bonding semiconductor packaging substrate 40, see figure 2A, column 4, lines 65 – column 5, line 1.

It would have been obvious to one having ordinary skill in this art at the time of the invention was made to have a wire-bonding semiconductor substrate as taught by Okabe et al. on the board of Kimura et al. for its simplicity and low potential cost.

6. Claims 12 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. (US 6806428).

Regarding claim 12, as shown in figures 6a-6i, Kimura et al. disclose a method of forming an electronic device on a library core for embedded passive components comprising:

(a) Providing an insulating core layer 31 (resin substrate) having an upper surface and a lower surface opposed to the upper surface, see column 4, lines 18-19;

(b) a plurality of openings 35 (penetration holes) penetrating therethrough, see column 4, lines 27-28;

(c) allowing the openings to be filled with capacitive material 37 (chip capacitors are made of capacitive material), see column 4, lines 30-32; and

(d) electrically conductive layers 32 (copper foil) are formed over the upper and lower surfaces of the core layer, see column 4, lines 17-24;

(e) patterning the electrically conductive layers respectively on the upper and lower surfaces of the core layer to form a plurality of the conductive traces 34 for electrically interconnecting the capacitive material contained in the openings of the core layer as well as partly used as parallel sheets onto the capacitive material to thereby form the library core with the embedded capacitors, see column 4, lines 25-53; and

(f) mounting and electrically connecting the library core with the embedded capacitors to the electronic device, see column 2, lines 54-58.

Kimura et al. disclose all of the limitations of the claimed invention to form of the final product except for the step of the openings being made before the electrically conductive layers are formed on the substrate. However, the step is not necessitating when the final product is being made. Therefore, it would have been obvious to one

having ordinary skill in the art at the time of the invention was made to provide the insulating core layer 31 being formed with the plurality of openings 35 before the forming of the electrically conductive layers 32 (formed into circuit pattern 34) in order to accurately connect the circuit pattern 34 for surely electrical connections between the wiring pattern 34 and the capacitor 37 and to prevent misalignment of the capacitor's electrodes and the wiring pattern.

Regarding claim 17, Kimura et al. disclose a plurality of conductive vias 33 for interconnecting the conductive layers on the upper and the lower surfaces of the core layer, see figure 6(b), column 4, lines 22-25.

Regarding claims 18, Kimura et al disclose a semiconductor packaging substrate 7 as the electronic device, see figure 1 and column 2; lines 54-58.

Response to Arguments

7. Applicant's arguments filed 12/15/05 have been fully considered but they are not persuasive. Applicant argues:

(a) Page 5, 4th paragraph: The arguments about a step in which Kimura et al. form the wiring pattern first before forming the holes and the inserting passive chips while the applicant forms the substrate with holes first before forming the wring pattern.

The examiner has considered the step is not necessitating when the final product is being made, see claim 12 above.

(b) Page 6, second paragraph: The arguments about the capacitor chips instead of capacitive material.

The examiner remarks, as shown in claim 1 above, disclose the capacitive material.

(c) Page 6, second paragraph: The arguments about the conductive layers formed as a whole on the core layer.

Claims 1 and 12 do not state such the limitation.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoa C. Nguyen whose telephone number is 571-272-8293. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hoa C. Nguyen
6/12/06